UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/392,034	09/08/1999	FERNANDO GONZALEZ	11675.119.1	9481

22901 7590 05/03/2002

JESUS JUANOS I TIMONEDA
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

EXAMINER
MAI, ANH D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/392,034	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27,31-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,31-40,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 2-4 are objected to under 37 CFR 1.75(c) for being of improper dependent form for failing to further limit the subject matter of a previous claim, **as previously applied**.

2. The amendment filed August 13, 2001 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure, **as previously applied**.

3. Claims 1-17, 42 and 43 are rejected under 35 U.S.C. 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, **as previously applied**.

4. Claims 1-4, 6, 7, 11 and 38 are rejected under 35 U.S.C. 102(e) for being clearly anticipated by Omid-Zohoor et al. (U.S. Patent No. 6,184,108), **as previously applied**.

5. Claim 43 is rejected under 35 U.S.C. 102(e) for being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072), **as previously applied**.

6. Claim 5 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '108 as applied to claim 1 above and further in view of Poon et al. (U.S. Patent No. 5,387,540), **as previously applied**.

7. Claim 8 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '108 as applied to claim 7 above, and further in view of Omid-Zohoor '072, **as previously applied**.

8. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '108, **as previously applied.**

9. Claims 14-17 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '108 in view of Poon et al. (U.S. Patent No. 5,387,540), **as previously applied**.

10. Claims 18, 19 and 24-27 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072, **as previously applied**.

11. Claims 20-22 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072, as applied to claim 18 above, and further in view of Lee '316, **as previously applied**.

12. Claim 23 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 21 above, and further in view of Poon '540, **as previously applied**.

13. Claims 31, 32 and 34 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316, **as previously applied**.

14. Claim 33 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 31 above, and further in view of Poon '540, **as previously applied**.

15. Claims 35-37 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '108 in view of Lee '316, **as previously applied**.

16. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '108 as applied to claim 38 above, and further in view of Lee '316, **as previously applied**.

17. Claim 42 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316, **as previously applied**.

Response to Amendment

1. The amendment filed February 14, 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "and said depositing is carried out to the extent of leaving no gap in each said isolation trench" and "said planarizing is performed in the absence of masking the conformal layer over each said isolation trench" and "liner being confined within each said isolation trench".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1-27, 31-40, 42 and 43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "depositing is carried out to the extent of leaving no gap in each said isolation trench" in the application as filed.

The specification as originally filed, fails to provide support for such a deposition.

Further, there does not appear to be a written description of the claim limitation "planarizing is performed in the absence of masking the conformal layer over each said isolation trench" in the application as filed. The same had been rejected in the previous Office Action.

2. Claims 4, 16 and 21 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "rounding the top edge of the trench" by thermally grown oxide from the substrate, does not reasonably provide enablement for rounding the top edge of trench by **depositing material** on the trench surface. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The specification clearly indicated that the rounding of the edge at the top of the isolation trench is a result of thermal oxidizing of the sidewall 50 to form the insulation liner 30. (See page 12, 1st paragraph). Further, as an alternative, the insulation liner can be formed by CVD.

The specification *fails to provide support* for rounding the top edge of the trench by depositing material.

It is well known in the semiconductor technology that by consuming silicon at the corner during the thermal growing the oxide liner, the top edge of the trench becomes rounded.

Deposition, e.g. CVD, on the other hand, does not consume any material from the silicon substrate. Therefore, rounding does not occur.

How can the edge of trench be rounded when no silicon is consumed ? (See Wolf).

3. Claims 14-17 and 21-23 are further rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for forming a thermal liner oxide 30 to be confined within each isolation trench, but does not reasonably provide enablement for depositing CVD, the liner 30 to be confined within each isolation trench. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

How can a dielectric material only be deposited within the trench ?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-26 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

What is the limitation "wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches" (claims 1, 7, 14, 18, 24, 25, 26 and 31) or "wherein electrically insulative material extends continuously between and within said plurality of isolation trenches" (claim 35 and 38) referring to ?

The "material and electrically insulative material" lacking antecedent, thus making the claims indefinite.

5. Claims 21-23 are further rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites the limitation "wherein said conformal third layer is composed of an electrically conductive material" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim.

The conformal third layer as disclosed in the specification is "isolation film 36" and "spacer 28 and isolation film 36 are made from the same material" and the material used to form the spacer 28 is dielectric material (TEOS). Thus, this layer does not appear to be electrically conductive material, but rather electrically insulative material. (See specification and other claims).

6. Claims 21-23 are furthermore rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 21-23 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification and claim 18, which claim 21 depends upon. In which, applicant has stated that the microelectronic structure is "isolation trench", and this statement indicates that the invention is different from what is defined in the claim(s) because to form an isolation trench, the trench fill material, e.g. conformal third layer should be electrically insulative material. Therefore, the limitation of claims 21-23 are in direct conflict with the invention "wherein said conformal third layer is composed of an electrically conductive material".

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor et al. (U.S. Patent No. 6,097,072) in view of S. Wolf, *Silicon Processing*.

As best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially similar as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer (340);

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

filling each isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344); and

planarizing the conformal layer (364) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces, wherein the planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of forming a thermal liner, e.g. rounding the top edge, of the isolation trench.

However, Wolf teaches that it is well known in the art to form a thermal liner on the etched trench surface, thus rounding the trench corner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top corner of the trench.

With respect to claims 2, 3 and 15, as best understood by the examiner, the liner of Wolf formed upon the sidewall of each isolation trench and is thermally grown oxide of the semiconductor substrate .

With respect to claim 4, as best understood by the examiner, the only way to round the top edge of the trench is thermally grown oxide from the substrate as taught by Wolf.

With respect to claims 5 and 14, as best understood by the examiner, Wolf further teaches that forming a doped region below the termination of each isolation trench within the semiconductor substrate.

With respect to claim 6, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor is formed by CMP.

With respect to claim 7, as best understood by the examiner, the method of Omid-Zohoor appears to further include planarizing the conformal layer with a single etch recipe; (See Fig. 3M);

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench (376), and being formed situated above the pad oxide layer (340); and

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the pad oxide layer (340). (See Fig. 3H).

With respect to claims 8 and 17, as best understood by the examiner, the method of Omid-Zohoor further includes:

removing the pad oxide layer (340) upon a portion of the surface of semiconductor substrate (120); and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

with respect to claim 9, 10 and 12, as best understood by examiner, Omid-Zohoor teach all of the features of the claim with the exception of explicitly disclosing that the etch rate of the conformal third layer (364) and the spacers (356) being faster than that of the first dielectric layer (344).

The selectivity rate of 1:1 to about 2:1 do not appear to be critical.

The CMP process of Omid-Zohoor '072 has resulted in a planar surface (Fig. 3M). The CMP process of Omid-Zohoor '072 is stopped when the silicon nitride (344) is exposed.

Further, it appears that the etch recipe of Omid-Zohoor '072 is at least including the claimed range because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces and such selective ratios are well known. (See Fig. 3M).

Given the teaching of the reference, it would have been obvious to one having ordinary skill in the art at the time of invention to use any etch recipe which comprises a higher removal rate of the oxide than the nitride layer to form a planar surface because as the polishing reaching the nitride layer, electrical or visual detection should be able to stop the polishing before over-etching occurred.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

With respect to claim 11, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor is formed including:

CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer. (See Figs. 3A-N).

8. Claims 18-22, 24, 26, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of S. Wolf, *Silicon Processing*.

With respect to claims 18 and 24, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially similar as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein the planarizing the conformal third layer (364) further comprises planarizing the conformal third layer (364) and each spacers (356) to form therefrom the co-planar upper surface, and the planarizing the conformal third layer is performed in the absence of masking the conformal third layer over the isolation trench; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of forming a thermal liner, e.g. rounding the top edge, of the isolation trench.

However, Wolf teaches that it is well known in the art to form a thermal liner on the etched trench surface, thus rounding the trench corner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top corner of the trench.

Further, although Omid-Zohoor does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, it is within the ability of a skilled worker in the art to recognize that the polysilicon layer, formed as an alternative, also removed to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention.

***

With respect to claim 19, as best understood by the examiner, the upper surface for each isolation trench of Omid-Zohoor is formed by CMP.

With respect to claims 20 and 31, as best understood by the examiner, Wolf further teaches that forming a doped region below the termination of each isolation trench within the semiconductor substrate.

With respect to claim 21, as best understood by the examiner, as taught by Wolf the liner oxide is formed upon the sidewall of the isolation trench prior to filling the isolation trench with the trench fill material.

Therefore, the method of Omid-Zohoor in view of Wolf further includes: prior to filling each isolation trench (360) with the conformal third layer (364), forming a liner upon the sidewall of the isolation trench, the liner being confined within each isolation trench and extending from an interface thereof with the oxide layer (340)to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer (364) is composed of an electrically insulative material.

With respect to claim 22, the liner of Wolf is a thermally grown oxide of the semiconductor substrate.

With respect to claims 26 and 27, a similar reasoning as that of claims 9, 10 and 12 is applied.

With respect to claim 32, as best understood by the examiner, each liner of Omid-Zohoor in view of Wolf is thermally grown oxide of the semiconductor substrate, and wherein the conformal layer (364) is composed of an electrically insulative material.

9. Claims 16, 23 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Wolf as applied to claims 21 and 31 above, and further in view of Poon '540.

Omid-Zohoor '072 and Wolf teach all of the features of the claim with the exception of forming liner comprises deposition of a composition of matter.

However, Poon teaches forming liner (50) upon sidewall (24) of isolation trench (22) comprises deposition of a composition of matter, silicon nitride. (See Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form liner of Wolf comprises deposition of a composition of matter as taught by Poon to protect the substrate form further oxidation.

With respect to claim 33, as best understood by the examiner, the conformal layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 34, as best understood by the examiner, method of Omid-Zohoor further includes:

exposing the oxide layer upon a portion of surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate;

forming between the isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of spacers (356); and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surface. (See Fig. 3O).

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of S. Wolf, *Silicon Processing.*

As best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially similar as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces, wherein the planarizing the conformal third layer is performed in the absence of masking the conformal third layer overreach of the isolation trenches;

exposing the oxide layer upon a portion of surface of the semiconductor substrate;

forming a gate oxide layer (380) upon a portion of the surface of the semiconductor substrate (120);

forming between the isolation trenches (376), and confined in the space therebetween a layer composed of polysilicon upon the oxide layer in contact with a pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of forming a thermal liner, e.g. rounding the top edge, of the isolation trench.

However, Wolf teaches that it is well known in the art to form a thermal liner on the etched trench surface, thus rounding the trench corner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top corner of the trench.

Further, although Omid-Zohoor does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, it is within the ability of a skilled worker in the art to recognize that the polysilicon layer, formed as an alternative, also removed to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention.

11. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of S. Wolf.

As best understood by the examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer;

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) and the polysilicon layer to expose the oxide layer at a plurality areas;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas, wherein electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of leaving no gap within each isolation trench and extending over the spacers (356) and over the first layer (344);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by planarizing in the absence of masking the second layer over each of the isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of forming a thermal liner, e.g. rounding the top edge, of the isolation trench.

However, Wolf teaches that it is well known in the art to form a thermal liner on the etched trench surface, thus rounding the trench corner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top corner of the trench.

Further, although Omid-Zohoor does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, it is within the ability of a skilled worker in the art to recognize that the polysilicon layer, formed as an alternative, also removed to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention.

With respect to claim 36, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 2-37).

With respect to claim 37, the width of the doped trench bottom of wolf is greater than the width of the respective isolation trench.

12. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of S.Wolf.

As best understood by the examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

selectively removing the first layer (344) to expose the oxide layer (340) at a plurality of areas;

forming a plurality of isolation trenches (360) through the oxide layer at the plurality of areas, wherein electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340); wherein the planar upper surface is

formed by planarizing in the absence of masking the second layer (364) over each of the isolation trench; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of rounding the top edge of the isolation trench.

However, Wolf teaches that it is well known in the art to form a rounded the trench top edge by forming a thermal liner on the etched trench surface.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form round the top edge of the trench (360) of Omid-Zohoor by forming a thermal liner on the surface of trench as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top corner of the trench.

With respect to claim 39, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of isolation trenches. (See Fig. 2-37).

With respect to claim 40, the width of the doped trench bottom of wolf is greater than the width of the respective isolation trench.

13. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of S. Wolf.

As best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a polysilicon layer upon the oxide layer;

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures (360), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of leaving no gap within each isolation trench and extending over the spaces (356) and the first layer (344); and

forming with a single etch recipe a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of rounding the top edge of the isolation trench.

However, Wolf teaches that it is well known in the art to form a rounded the trench top edge by forming a thermal liner on the etched trench surface.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form round the top edge of the trench (360) of Omid-Zohoor by forming a thermal liner on the surface of trench as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top edge of the trench.

Further, although Omid-Zohoor does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, it is within the ability of a skilled worker in the art to recognize that the polysilicon layer, formed as an alternative, also removed to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention.

14. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of S. Wolf.

As best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344);

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of leaving no gap within each isolation trench and extending over the spaces (356) and the first layer (344); and

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of respective first and second isolation

structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of rounding the top edge of the isolation trench.

However, Wolf teaches that it is well known in the art to form a rounded the trench top edge by forming a thermal liner on the etched trench surface.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form round the top edge of the trench (360) of Omid-Zohoor by forming a thermal liner on the surface of trench as taught by Wolf to remove silicon damage caused by the trench-etch step. Further, the growing of the thermal liner is inherently resulted in rounding the top edge of the trench.

Response to Arguments

15. Applicant's arguments filed February 14, 2002 have been fully considered but they are not persuasive.

Claim Objection:

By claiming "rounding the top edge" (claim 1) the limitation has indirectly included thermally grown oxide from the trench surface. The specification regarding "rounding of the top edge" clearly states: "[I] Fig. 5A it can be seen that, following thermal oxidation of sidewall 50

to form insulation liner 30 within isolation trench 32, semiconductor substrate 12 forms rounded edge at the top of isolation trench 32" (page 12, lines 4-6).

Therefore, the limitations: "further comprising forming a liner upon sidewall of each said isolation trench" (claim 2) and "wherein a liner is a thermally grown oxide of said semiconductor substrate" (claim 3) clearly do not further limit the subject matter has already claimed in claim 1, which these claims depend on.

The Objection therefore maintained.

Claim Rejection Under 35 U.S.C. 112, first paragraph:

Through a lengthy argument, applicant still fails to point out the specific disclosure regarding the planarizing is performed in the **absence** of masking the conformal layer, even the cited portion also fails as well.

Regarding the "single etch recipe", contrary to the applicant's conclusion, the term "the single etchbach uses an etch recipe" does not support the "single etch recipe".

Since the term "single etchback" referring to a process, while the term "single etch recipe" (claimed term) is referring to a chemical used in the etch.

The rejections are therefore, maintained.

Claim Rejection Under 35 U.S.C. 112, second paragraph:

First of all, to fully appreciate the invention, one should establish the term of the claim.

The spacer 28 of the specification is "spacer" in the claims.

The isolation film 36 (trench fill oxide) is "conformal layer" in the claims.

The "insulator island 22" (formed from nitride layer 16) is "first dielectric layer" in the claims.

As disclosed in the specification, page 14, lines 14-25, "[P]referably, planarization will be selective to isolation film 36 and relatively slightly selective to insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulation island 22".

A CMP is well known in the art, that a "hard" layer is used as an etch stop, because when the polishing reaches the "hard" layer, the operator, human or machine, should be able to detect that the intended material has been removed and the polishing is stopped. The above passage is crystal clear and fall in line with well known process.

The claim limitation on the other hand, recites: "an etch recipe that etches said first dielectric layer (insulator island 22) faster than said conformal layer (isolation film 36) and said spacers (spacer 28) by a ratio from about 1:1 to about 2:1".

Clearly, such limitation contradicting what was disclosed, thus, indefinite.

Furthermore, to achieve the "nail shape" the etch should stop at the surface of the insulator island 22, followed by a chemical etch (H_3PO_4) to remove island 22, thus leave the T-shape or nail-shape.

If etching according to the claimed limitation, which is not supported by the specification, the resulting upper surface should be at the top of the semiconductor substrate (12), thus, the nail-shape could not formed.

The applicant does not appear to appreciate his specification, cited portion, and invention.

To fully appreciate the scope of the instant invention and how the nail-shape isolation being formed, applicant is urged to review Pan et al. (U.S. Patent No. 5,763,932).

16. Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 27, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800